In the Claims:

This listing of claims replaces all prior versions.

1. (previously presented) A programmable audio processor chip for processing voice data comprising:

a DSP voice compression device adapted to compress the voice data;

audio processing circuitry programmed with an audio processing software application for processing the compressed voice data;

an IP network stack adapted to store and process IP data, the IP network stack including protocols for processing the compressed voice data via an IP network; and

a communication stack adapted to store and process communications data, the communications stack including audio processing protocols for processing the compressed voice data.

2. (previously presented) The programmable audio processor chip of claim 1, wherein the programmable audio processor chip is further adapted to convert the voice data between IP audio data and digital audio data.

3. (original) The programmable audio processor chip of claim 1, further comprising an analog-digital (A/D) converter adapted to convert the voice data between analog and digital form.

4. (previously presented) The programmable audio processor chip of claim 3, wherein the A/D converter is adapted to convert a voice signal captured at a microphone of a telephony device employing the programmable audio processor chip.

5. (previously presented) The programmable audio processor chip of claim 3, further comprising a telephony device that houses the programmable audio processor chip,

wherein the A/D converter is adapted to convert digital data into analog form for use at a speaker of the telephony device.

6. (previously presented) The programmable audio processor chip of claim 1, wherein the IP network stack includes at least one of: a TCP/IP stack and a H.323 stack.

7. (original) The programmable audio processor chip of claim 1, wherein the communication stack is adapted to provide at least one of the following protocols: call setup, call tear down, capabilities exchange and negotiation.

8. (previously presented) The programmable audio processor chip of claim 1, further comprising sufficient on-chip RAM to run a connection-less thin client call stack, a TCP/IP stack and audio compression protocols, wherein the programmable audio processor chip is adapted to function without external system memory.

9. (previously presented) The programmable audio processor chip of claim 1, wherein the programmable audio processor chip is adapted to dissipate 250 mW at 200 MHz.

10. (original) The programmable audio processor chip of claim 1, wherein the audio processing circuitry is programmed with a power-down mode, wherein the internal clock frequency is slowed during periods of chip inactivity.

11. (original) The programmable audio processor chip of claim 1, wherein the audio processing circuitry is adapted to be programmed using C programming language.

12. (original) The programmable audio processor chip of claim 1, wherein the audio processing circuitry further comprises Flash-cache architecture adapted to enable a CPU

to boot and run code from an external Flash-style device, and mix this execution space with memory on the chip.

13. (previously presented) A telephony communications device adapted to communicate data including voice data, the device comprising:

a programmable audio processor chip having both microcontroller and DSP functions and adapted to perform Internet protocol/digital (IP/D) conversions for IP voice data and digital voice data, wherein the programmable audio processor chip includes an IP network stack and a communications stack;

an audio capture device communicatively linked to the programmable audio processor chip and adapted to capture a voice signal and communicate the captured voice signal to the programmable audio processor chip; and

an audio speaker communicatively linked to the programmable audio processor chip and adapted to generate sound in response to a signal communicated from the programmable audio processor chip.

14. (previously presented) The telephony communications device of claim 13, wherein the programmable audio chip comprises:

a DSP voice compression device adapted to compress the voice data;

audio processing circuitry programmed with an audio processing software application for processing the compressed voice data;

the IP network stack adapted to store and process IP data, the IP network stack including protocols for processing the compressed voice data via an IP network; and

the communication stack adapted to store and process communications data, the communications stack including audio processing protocols for processing the compressed voice data.

15. (previously presented) The telephony communications device of claim 13, wherein the telephony communications device further comprises flash-style, non-volatile

memory that includes embedded firmware for that device, and wherein the programmable audio processor chip includes a flash-cache architecture adapted to enable a CPU to boot and run code from the Flash-style, non-volatile memory and mix this execution space with internal memory on the programmable audio processor chip.

16. (previously presented) The telephony communications device of claim 15, further comprising a plurality of communications stacks, wherein the device is adapted to run compute-intensive DSP code out of the internal memory and to run the communication stacks out of the flash-style, non-volatile memory.

17. (previously presented) The telephony communications device of claim 16, wherein the device is adapted to run the compute-intensive DSP code including at least one of: audio codecs, acoustic echo cancellation and framing.

18. (original) The telephony communications device of claim 16, wherein the communication stacks are adapted to process data for executing at least one of: call setup, call teardown, capabilities exchange and negotiation.

19. (canceled)

20. (previously presented) An IP telephony communications network comprising:

a plurality of IP telephony devices each having a programmable audio processor chip comprising:

a DSP voice compression device adapted to compress the voice data;

audio processing circuitry programmed with an audio processing software application for processing the compressed voice data;

an IP network stack adapted to store and process IP data, the IP network stack including protocols for processing the compressed voice data via an IP network; and

a communication stack adapted to store and process communications data, the communications stack including audio processing protocols for processing the compressed voice data;

a CPU adapted to communicate with the plurality of IP telephony communications devices and to program the programmable audio processor chip in each IP telephony device, the programming including communications protocols, the CPU having a standard RISC 5-stage pipeline adapted to execute a plurality of instructions simultaneously; and

a communications link coupled to each of the IP telephony devices and to the CPU and adapted to transmit communications data including voice IP data.

21. (original) The network of claim 20, wherein the CPU further comprises a DSP Multiply Accumulate (DSPMAC) unit and an Address Generation Unit (AGU).

22. (original) The network of claim 21, wherein the AGU is adapted to effect address calculation concurrently with normal program flow address calculation of the CPU.

23. (previously presented) An IP telephony communications network comprising:

a plurality of IP telephony devices each having a programmable audio processor chip comprising:

a DSP voice compression device adapted to compress the voice data;

audio processing circuitry programmed with an audio processing software application for processing the compressed voice data;

an IP network stack adapted to store and process IP data, the IP data including protocols for processing the compressed voice data via an IP network; and

a communication stack adapted to store and process communications data, the communications data including audio processing protocols for processing the compressed voice data;

a CPU adapted to communicate with the plurality of IP telephony communications devices and to program the programmable audio processor chip in each IP telephony device, the programming including communications protocols, the CPU having a standard RISC 5-stage pipeline adapted to execute a plurality of instructions simultaneously, a DSP Multiply Accumulate (DSPMAC) unit and an Address Generation Unit (AGU), the AGU adapted to effect address calculation concurrently with normal program flow address calculation of the CPU, the DSPMAC and AGU being adapted to be used together in single instruction mnemonics; and

a communications link coupled to each of the IP telephony devices and to the CPU and adapted to transmit communications data including voice IP data.

24. (previously presented) The programmable audio processor chip of claim 1, wherein the IP network stack includes at least one of: a TCP/IP stack and an IP telephony stack.

25. (previously presented) A programmable audio processor chip for processing telephony voice data comprising:

a DSP voice compression and decompression device adapted to compress and decompress the telephony voice data;

a programmable processing layer programmed with an audio processing application for processing the compressed telephony voice data;

an IP network stack adapted to store and process IP telephony data, the IP network stack including protocols for processing the compressed telephony voice data via an IP network; and

a communication stack adapted to store and process communications data, the communications stack including audio processing protocols for processing the compressed voice data.

26. (previously presented)The programmable audio processor chip of claim 25, further comprising an application layer programmed using C programming language.

27. (previously presented)The programmable audio processor chip of claim 26, wherein the application layer is adapted for programming with assembly language.

28. (previously presented) The programmable audio processor chip of claim 25, wherein the DSP voice compression and decompression device is an executable function on the programmable audio processor chip coded as assembly language.